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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,633	01/24/2001	Shota Iwasaki	NECN 18.280	3961
7590	10/31/2003			
Katten Muchin Zavis Rosenman 575 Madison Avenue New York, NY 10022-2585			EXAMINER	
			PATEL, ISHWARBHAI B	
			ART UNIT	PAPER NUMBER
			2827	

DATE MAILED: 10/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/768,633	IWASAKI ET AL.
	<b>Examiner</b> Ishwar (I. B.) Patel	<b>Art Unit</b> 2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply is specifically specified above, it will expire after the later of three months or thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on July 8, 2003 (amendment).
  - 2a) This action is **FINAL**.                    2b) This action is non-final.
  - 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.
- Disposition of Claims** *3-8* *10-11*
- 4) Claim(s) 1 and 2 is/are pending in the application.
  - 4a) Of the above claim(s) 4-8 is/are withdrawn from consideration.
  - 5) Claim(s) \_\_\_\_\_ is/are allowed.
  - 6) Claim(s) 1 and 3 is/are rejected.
  - 7) Claim(s) \_\_\_\_\_ is/are objected to.
  - 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 24 January 2003 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
  - a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: \_\_\_\_\_

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaji et al., US Patent No. 6,198,165, hereafter, Yamaji, in view of Tokuda Hiroshi, Japanese Patent No. JP403045398A.

Regarding claim 1, Yamaji discloses a single circuit board comprising:  
a base member (insulating substrate 6, see figure 1 and 2, column 6, line 7-10),  
an interconnect layer formed on a part of the base member (wiring pattern 8, see figure 1 and 2, column 7, line 10-15),

an electrically-floating conductive layer formed on a substantially remaining part of the base member and having an edge adjacent to an edge of the interconnect layer (dummy wiring pattern 14, see figure 1 and 2, column 7, line 10-15), and

a dielectric layer covering a part of the interconnect layer and an entire surface of the electrically-floating conductive layer, and filling a gap between the edge of the interconnect layer and the edge of the electrically-floating conductive layer (a solder resist 7, see figure 1 and 2, column 6, line 7-10), but

fails to disclose a bottom interconnect layer on a bottom surface of the base member and a bottom electrically floating conductive layer on the bottom surface of the base member.

Tokuda discloses a circuit board with interconnect layers and a floating layers on the both sides of the base member.

Further, double sided circuit boards or multilayer circuits board are known in the art to increase the component density by installing the component on both the side of the circuit board or installing the components on one side and connecting the other surface to another board, such as mother board along with floating layer to provide shielding.

A person of ordinary skill in the art will use the knowledge available in art to increase the component density depending upon the specific applications.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of Yamaji with the interconnect layer and the floating layer on both surface of the board, as taught by Tokuda, in order to increase the component density and at same time provide shielding to reduce the disturbances.

Regarding claim 3, the applicant is claiming a volume of the top interconnect layer and a volume of the bottom interconnect layer substantially equal.

Though, the combination of Yamaji and Tokuda does not explicitly disclose the volume of the top interconnect layer and the volume of the bottom interconnect layer

substantially equal, the volume of the interconnect layer will depend upon the thickness of the interconnect layer, density of the traces and connection pads and the routing of the traces for the specific applications.

As disclosed by Tokuda, the important criteria are to control the volume of the conductive material on both the side of the board to balance the stress and avoid warpage.

A person of ordinary skill in the art will control the volume of conductive material on both the side of the circuit board, either by providing the same volume of interconnect and floating layer on both the side, if possible, or adjust the respective volume of interconnect and floating layer on both the side to control stress and avoid warpage of the board.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of Yamaji with the volume of the top interconnect layer and the volume of the bottom interconnect layer substantially equal, as taught by Tokuda, in order to avoid stress and warpage.

***Response to Arguments***

3. Applicant's arguments with respect to claims 1 and 3 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mark et al., discloses a circuit board with both top and bottom surfaces covered with conductive layers except the component-connecting region.

Matsumoto et al., discloses a double sided circuit board with the volume of the conductive material on both the surface controlled by providing slits 5 in the dense circuit area, see figure 1.

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (703) 305 2617. The examiner can normally be reached on M-F (8:30 - 5).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703) 308 1233. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305 3900.

  
ERNEST J. KARLSEN  
PRIMARY EXAMINER

ibp